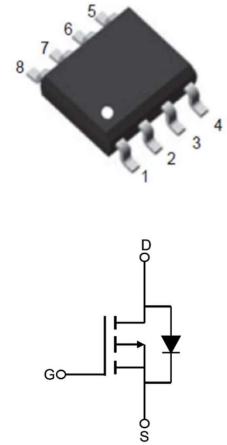
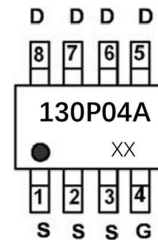


**P-CHANNEL ENHANCEMENT MODE POWER MOSFET****PRIMARY CHARACTERISTICS**

BV _{DSS}	R _{DS(on)} MAX	I _D
-40V	14.3mΩ@V _{GS} =-10V	-40A
	22mΩ@V _{GS} =-4.5V	

SCHEMATIC DIAGRAM**SOP-8 PACKAGE**

Marking :

**GENERAL DESCRIPTION**

- Advanced Trench Technology.
- Excellent RDS(ON) and Low Gate Charge.
- Lead free product is acquired.

MECHANICAL DATA

- Case : Molded plastic,SOP-8
- Polarity : Shown above
- Terminals :Plated terminals, solderable per MIL-STD-750,Method 2026
- Epoxy : UL94-V0 rated flame retardant

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Symbol	Parameter		Max.	Units
V _{DSS}	Drain-Source Voltage		-40	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Continuous Drain Current	T _A = 25°C	-40	A
		T _A = 100°C	-26	A
I _{DM}	Pulsed Drain Current ^{note1}		-160	A
E _{AS}	Single Pulsed Avalanche Energy ^{note2}		144	mJ
P _D	Power Dissipation	T _A = 25°C	40	W
R _{θJA}	Thermal Resistance, Junction to Ambient		3.1	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C



P-CHANNEL ENHANCEMENT MODE POWER MOSFET

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

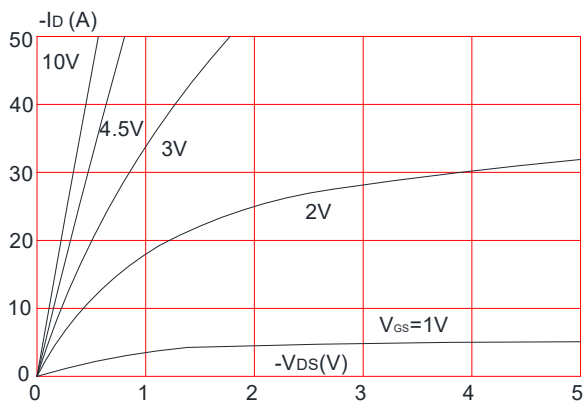
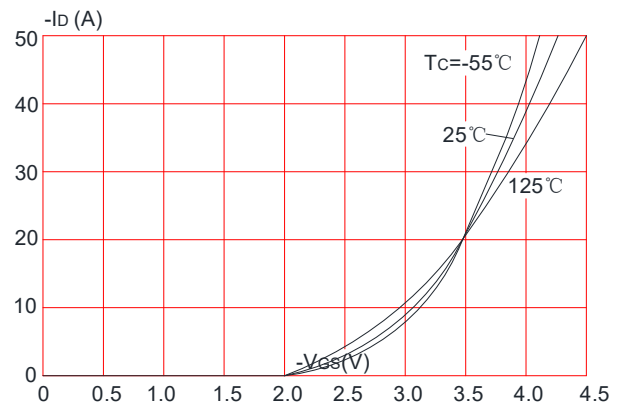
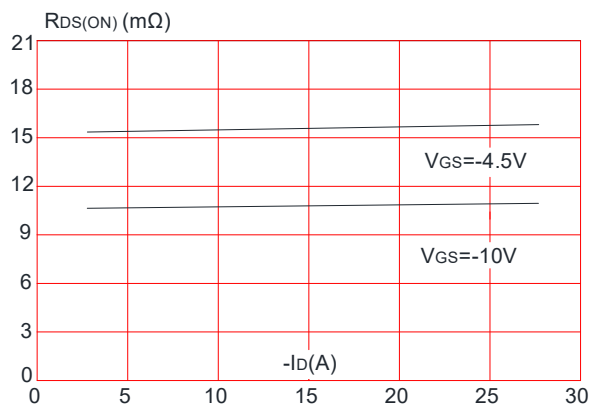
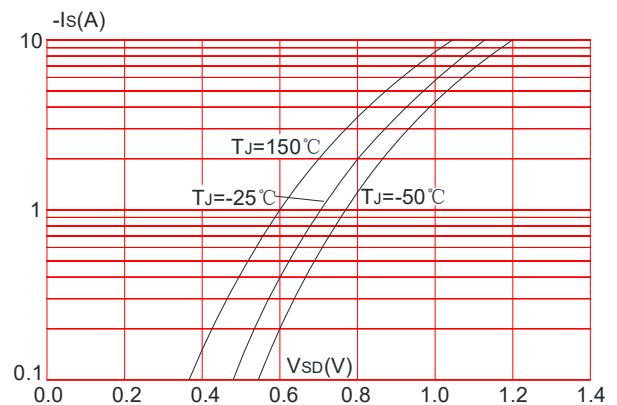
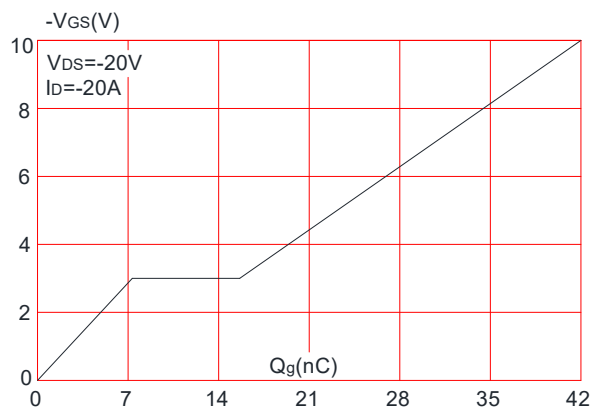
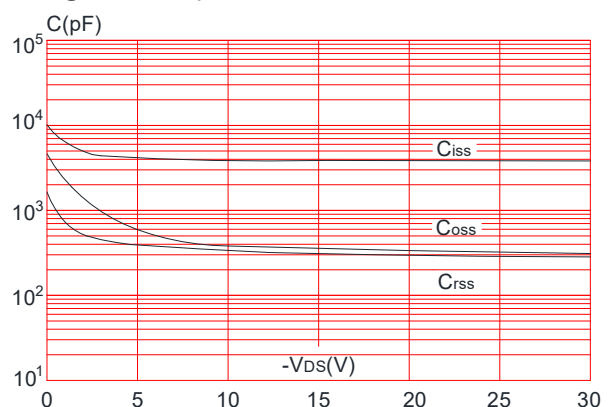
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.7	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} = -10V, I _D = -20A	-	11	14.3	mΩ
		V _{GS} = -4.5V, I _D = -10A	-	15.5	22	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	3800	-	pF
C _{oss}	Output Capacitance		-	329	-	pF
C _{rss}	Reverse Transfer Capacitance		-	289	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -20A, V _{GS} = -10V	-	42	-	nC
Q _{gs}	Gate-Source Charge		-	7.3	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	8.5	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -20A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	10	-	ns
t _r	Turn-on Rise Time		-	21	-	ns
t _{d(off)}	Turn-off Delay Time		-	53	-	ns
t _f	Turn-off Fall Time		-	29	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-40	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-160	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -30A	-	-0.8	-1.2	V
trr	Reverse Recovery Time	V _{GS} =0V, I _S = -30A,	-	39	-	ns
Qrr	Reverse Recovery Charge	di/dt=100A/μs	-	42	-	nC

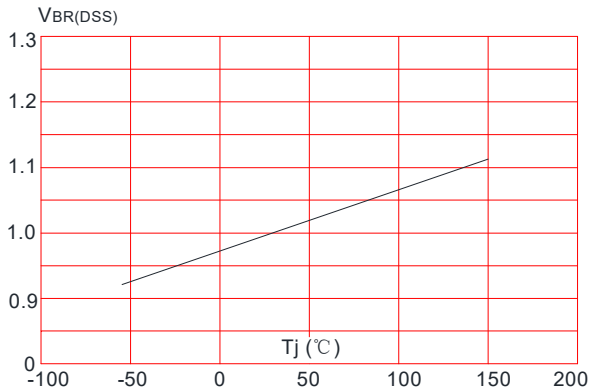
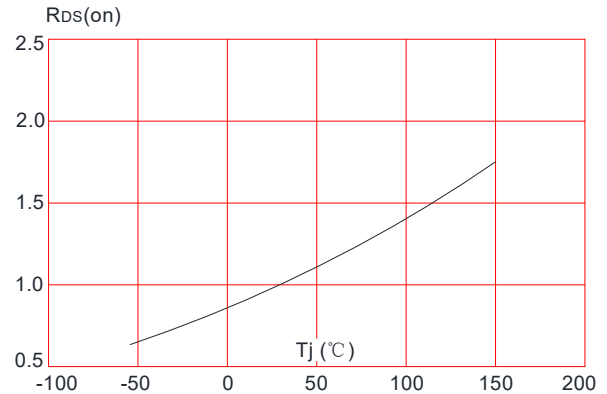
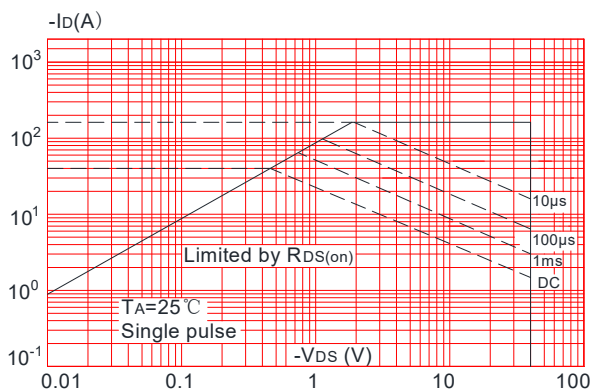
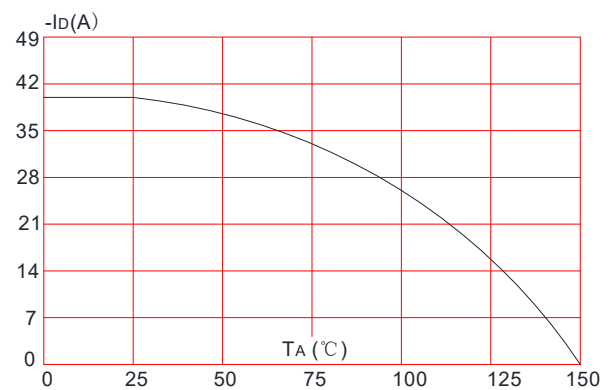
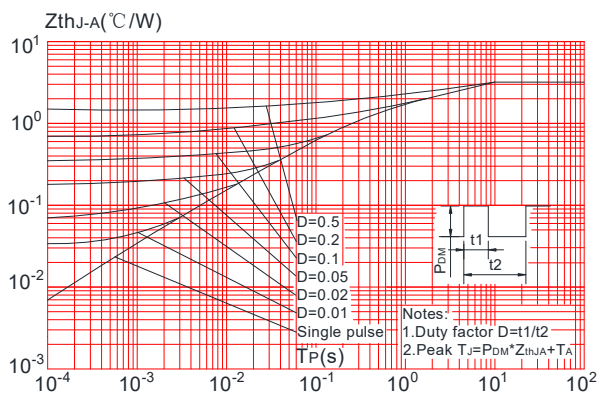
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=-20V$, $V_G=-10V$, $L=0.5mH$, $R_G=25\Omega$, $I_{AS}=-24A$ 3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



Typical Performance Characteristics

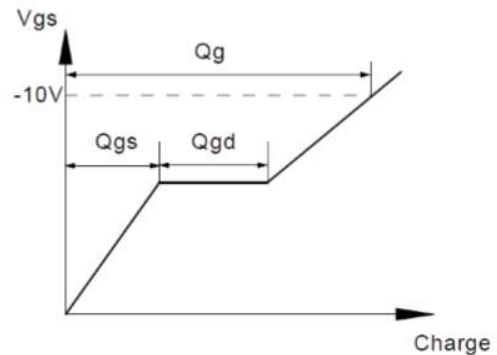
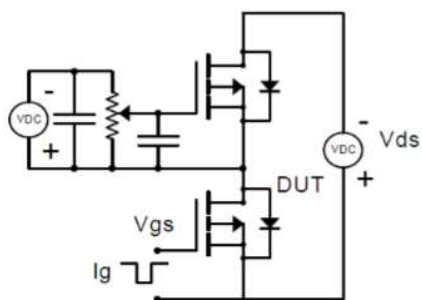
Figure1: Output Characteristics**Figure 2: Typical Transfer Characteristics****Figure 3: On-resistance vs. Drain Current****Figure 4: Body Diode Characteristics****Figure 5: Gate Charge Characteristics****Figure 6: Capacitance Characteristics**

**P-CHANNEL ENHANCEMENT MODE POWER MOSFET****Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature**Figure 8:** Normalized on Resistance vs. Junction Temperature**Figure 9:** Maximum Safe Operating Area**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

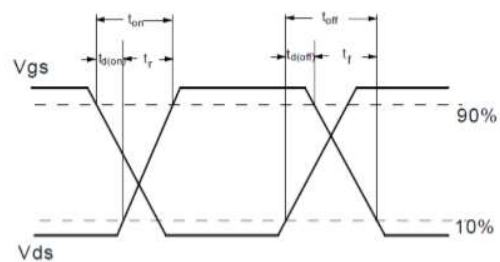
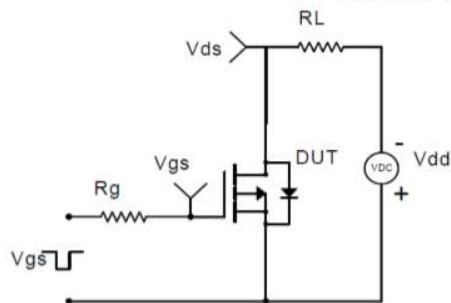


Test Circuit

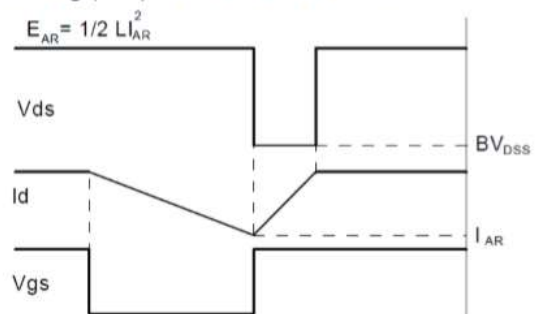
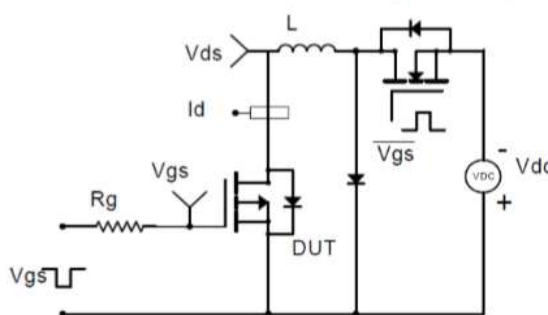
Gate Charge Test Circuit & Waveform



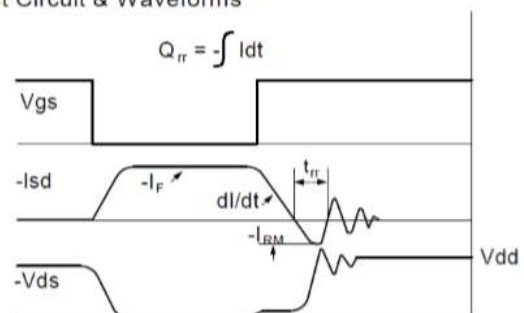
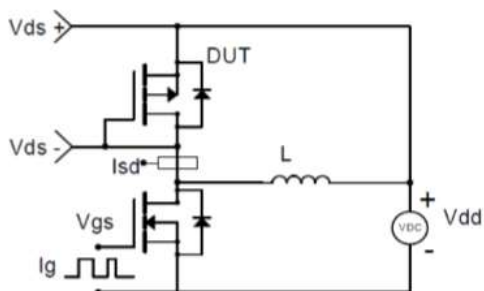
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



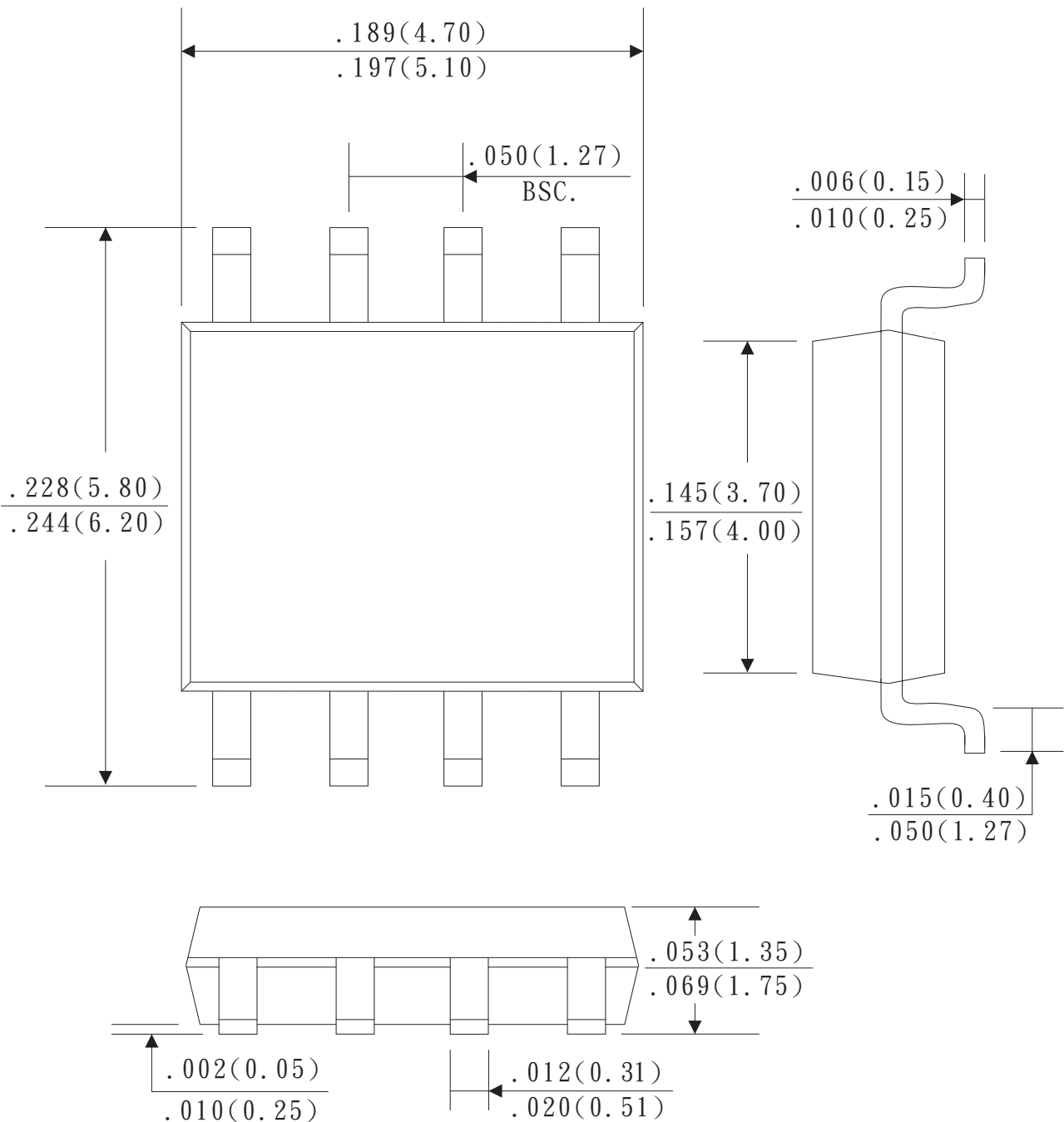
Diode Recovery Test Circuit & Waveforms





Outline Drawing

SOP-8



Dimensions in inches and (millimeters)

Rev.E

**Ordering Information:**

Device PN	Packing
SEQ130P04A -T ⁽¹⁾ H ⁽²⁾ -WS ⁽³⁾	Tape&Reel: 4 Kpcs/Reel

Note: (1) Packing code, Tape & Reel Packing

(2) Halogen free product for packing code suffix "H"

(3) Willas brand abbreviation, Label Type does not display

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